

rejected as anticipated by the patent to Shimanuki. Claim 15 has been rejected as anticipated the patent to Kotooka, et al.. Each of these claims have been cancelled and accordingly these rejections are considered obviated.

Claim 1 has been rejected as unpatentable over Iida, et al. The Examiner stated that Iida, et al. teaches that a singled crystal ingot of silicon was pulled while varying the average pulling rate over a range of 1.0 mm/min and 0.4 mm/min. The Examiner stated that it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Iida, et al. by attempting to optimize the temperature range by conducting routine experimentation. Applicant will assume that the Examiner has meant to also reject claims 4 and 5 over Iida, et al. as well, although such is not explicitly stated.

Iida, et al. uses $\Delta G = G_e - G_c$ where G_e equals the temperature at a peripheral portion of the crystal and G_c is the temperature at the center of the crystal. The furnace temperature of Iida, et al. is adjusted so that ΔG is controlled to be within $5^\circ\text{C}/\text{Cm}$. The use of the ratio $G_{\text{edge}} - G_{\text{center}}$ as parameters is different from the use of the differential $G_e - G_c$ as parameters and is not obvious therefrom.

In further explanation, in the subject invention, the defect seed in the crystal is determined from the V/G_1 value and the distribution of the defect seeds in the diameter direction is determined by the value of $((V/G_1)_{\text{edge}} / ((V/G_1)_{\text{center}})$ (=assumed to be R) and the value of $(V/G_1)_{\text{center}}$ of the crystal center. Here, considering one crystal, since the pulling speed V is identical for the edge and the center, it can be expressed as:

$$R = G_{1_{\text{edge}}} / G_{1_{\text{center}}} \rightarrow G_e / G_c \dots (1)$$

When $Gle/Glc = K$ is used as a parameter, then it can be expressed as $Gle = k \cdot Glc$... (2)

When substituting the equation (2) for the equation (1), it becomes $R = (k \cdot Glc)/Glc - k$... (3)

which holds a relation $R = k$.

The Iida, et al invention uses $\Delta G = Gle - Glc = d$ as a parameter (0/10, lines 45-55).
In this case, it can be expressed as

$$Gle = d + Glc \text{ ... (4)}$$

When substituting the equation (4) for the equation (1), it becomes
 $R = (d + Glc)/Glc = 1 + (d/Glc)$... (5)

which does not equate to the $R = d$.

According to the present invention, because the value of R is determined regardless of the temperature gradient Glc on the crystal center axis, it is possible to determine the distribution of defect seeds by Gle/Glc . However, the defect seed in the center portion is determined by the absolute value of Glc , which is expressed by the OSF ring (inner diameter/crystal diameter) in the present invention.

According to the Iida, et al. invention, the value of R varies depending on Glc . Even if it is identical, R becomes large when Glc is small. Therefore, the difference between the character of the defect seed in the portion and the character of the defect seed in the periphery portion is generally large. In practice, the value of R greatly changes according to the environmental change in the furnace, e.g., alteration of the in-furnace carbon parts, etc., or the pulling speed. Thus, it can be seen that Iida, et al.'s theory of

invention and approach to the problem of preventing crystal defects is radically different for that of Applicants', which therefore cannot be obvious from the teachings of Iida, et al.

Claim 1 has also been rejected as unpatentable over the patent to Hourai, et al. The Examiner stated that it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Hourai, et al. by attempting to optimize the temperature range by conducting routine experimentation. Hourai, et al. uses the V/G value of the crystal center position and the V/G value of the outer perimeter as parameters from which to make silicon single wafers free of grown-in defects. The Examiner stated that " it would have been obvious to modify Hourai by deriving the condition of claim 1 based on the profile of Figure 2". However, Figure 2 makes no mention of a parameter based on a temperature of the crystal on the outer surface in a ratio with the temperature of the crystal on the inner surface. Since Hourai, et al. does not even contemplate the temperature of the crystal at the outer surface of the crystal, Figure 2 cannot be used to teach or suggest the method of the subject invention. Applicants will assume that claims 3, 4 and 5 have also been rejected based on Hourai, et al., although there is no explicit rejection in the Office Action.

As claims 3, 4 and 5 are dependant on claim 1, the above arguments hold true for these claims as well.

Claim 6 has been rejected as unpatentable over the patent Luter, et al. Claim 6 has been cancelled above and accordingly this rejection is considered obviated.

Claim 7 has been rejected as unpatentable over the patent Kim, et al. in view of Luter, et al. Applicants have amended claim 7 so that it now recites the ratio V/G and the ratio G outer/G center, parameters which are not taught by Kim, et al. or Luter, et al. or the other art of record. Accordingly, claim 7 is considered patentable.

Claims 9-11 have been rejected as being unpatentable over the patent to Adachi, et al. The Examiner has stated that "it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Adachi, et al. by attempting to optimize the same by conducting routine experimentation. Adachi, et al. (col. 10, lines 65-67) teaches that in order to form a defect-free crystal, annealing should be performed by heating from 500°C to 900°C at a rate of between 0.5°C/min and 5°C/min. However, Adachi, et al. does not suggest a heat treatment temperature at the initial entry at 500°C or less.

As shown in Figure 8 of the present invention, by setting the heat treatment temperature at an initial entry 500°C or less, it is possible to equalize the distribution of the oxide precipitate density. As Adachi, et al. does not suggest such a temperature, claims 9-11 are patentable thereover.

Claims 14, 17 and 21 have been rejected as unpatentable over Kotooka, et al. in view of Shimanuki, et al. Further, claim 16 has been rejected as unpatentable over Kotooka, et al. in view of Hourai, et al. and claims 18-20 have been rejected as unpatentable over Kotooka, et al. Further, claim 23 has been rejected as unpatentable over Wijaranakula, et al. in view of Hourai, et al. By the cancellation of claims 14-23, this rejection is considered obviated.

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Applicants hereby request reconsideration and re-examination thereof.

With the above Amendments and remarks this application is considered ready for allowance and Applicants earnestly solicit an early notice of same. Should the Examiner be of the opinion that a telephone conference would expedite prosecution of the subject application, he is respectfully requested to call the undersigned at the below-listed number.

No further fee or petition is believed to be necessary in addition to those that are enclosed. Should any fee be needed, please charge our Deposit Account No. 23-0920, and deem this paper to be the required petition.

Respectfully submitted,

By: Gerald T. Shekleton
Gerald T. Shekleton, Reg. No. 27,466

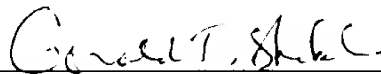
WELSH & KATZ, LTD.
120 South Riverside Plaza, 22nd Floor
Chicago, Illinois 60606
Phone (312) 655-1500
Fax No. (312) 655-1501

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CERTIFICATE OF MAILING

I hereby certify that this Amendment and a Postcard are being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to Attention: Box Amendment, Commissioner for Patents, Washington, D.C. 20231, on August 28, 2002.

A handwritten signature in cursive script, reading "Gerald T. Shekleton", written over a horizontal line.

Gerald T. Shekleton

Claims with markings to show amendments

7. (Amended) A Czochralski method-based silicon single crystal production device, comprising, in a closed container, a crucible element which stores silicon melt, rotates and is vertically driven, a pulling element for pulling a silicon crystal ingot, while rotating, from said silicon melt, a heating element for heating said crucible, [element] and a heat shielding element for shielding radiating heat from said heating element, characterized in that a drive mechanism for moving said heat shielding element is equipped for changing an in-crystal temperature gradient in a pulling axis direction of the silicon crystal ingot and for adjusting a ratio V/G of a pulling speed V in the Czochralski method to an average value G of the in-crystal temperature gradient in a pulling axis direction within a temperature range from the silicon melting point to 1350°C to be within a range of 0.16 to $0.18 \text{ mm}^2/^{\circ}\text{C min.}$ and a ratio $G_{\text{outer}}/G_{\text{center}}$ is 1.10 or less, where G_{outer} and G_{center} are the temperature at the crystal outer surface and the temperature at the crystal center respectively.

9. A heat treating method for a silicon single crystal wafer related to a perfect crystal produced by a Czochralski method, characterized in that a heat treatment temperature at the initial entry of the silicon single crystal wafer to be a target of the heat treatment is 500°C or less, and a temperature ramping rate in a temperature range from the heat treatment temperature at initial entry to an ultimate temperature set in a range of $[]700^{\circ}\text{C} - 900^{\circ}\text{C}[]$ is set to 1°C/min or less.

10. A heat treating method for a silicon single crystal wafer related to a perfect crystal produced by a Czochralski method, characterized in that a heat treatment temperature at the initial entry of the silicon single crystal wafer to be a target of the heat treatment is 500°C or less, and a temperature ramping rate in a temperature range from the heat treatment temperature at initial entry to an ultimate temperature set in a range of ["]700°C - 900°C ["] is set to 1°C/min or less, so as to make uniform the distribution of an oxide precipitate density of the silicon single crystal wafer after heat treatment

11. A heat treating method for a silicon single crystal wafer related to a perfect crystal produced by a Czochralski method, characterized in that a heat treatment temperature at the initial entry of the silicon single crystal wafer to be a target of the heat treatment and a temperature ramping rate from the heat treatment temperature at initial entry to an ultimate temperature set in a range of ["]700°C - 900°C["] are adjusted so as to adjust the distribution of an oxide precipitate density of the silicon single crystal wafer after heat treatment.